AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) A method for providing redundancy when field programming ~~writing to~~ a memory array, the method comprising:

(a) providing a memory array comprising a primary block of memory cells and a redundant block of memory cells; ~~and~~

(b) attempting to field program the primary block with data;

(c) detecting an error in field programming the primary block with the data; and

(~~b~~d) in response to detecting the error ~~an error in writing to the primary block when field programming the memory array~~:

(~~b~~d1) field programming ~~storing~~ a flag in a set of memory cells allocated to the primary block, wherein the set of memory cells is in the memory array; and

(~~b~~d2) field programming ~~writing to~~ the redundant block with the data;

wherein the flag indicates that the redundant block should be read instead of the primary block to read the data.

2. (Currently Amended) The invention of Claim 1 further comprising:

(~~c~~e) in response to a command to read the primary block, reading the set of memory cells allocated to the primary block; and

(~~d~~f) in response to reading the flag stored in the set of memory cells allocated to the primary block, reading the redundant block.

3. (Currently Amended) The invention of Claim 1, wherein the primary block comprises a plurality of smaller blocks, and wherein the error in ~~writing to~~ field programming the primary block occurs when there is an error in ~~writing~~ field programming at least one bit in one of the smaller blocks.

4. (Original) The invention of Claim 3, wherein the smaller block comprises an oct-byte and the primary block comprises a page.

5. (Currently Amended) The invention of Claim 1, wherein the error occurs when there is an error in ~~writing~~ field programming a single bit.

6. (Currently Amended) The invention of Claim 1, wherein the error occurs when there is an error in ~~writing~~ field programming two bits.

7. (Currently Amended) The invention of Claim 1, wherein the error occurs when there is an error in ~~writing~~ field programming X bits, wherein X is sufficient to introduce an error that is uncorrectable by an error protection scheme protecting at least some of the memory cells in the primary block.

8. (Currently Amended) The invention of Claim 1, wherein (c) comprises ~~further comprising determining the error occurred by~~:

attempting to field program a memory cell in the primary block; and

while attempting to field program the memory cell, determining that the memory cell is not in a programmed state.

9. (Currently Amended) The invention of Claim 1, wherein (c) comprises ~~further comprising determining the error occurred by~~:

attempting to field program a memory cell in the primary block;

reading the memory cell after the attempt to field program the memory cell; and

determining that the memory cell is not in a programmed state.

10. (Original) The invention of Claim 1, wherein the primary block is associated with the redundant block via direct mapping.

11. (Original) The invention of Claim 1, wherein the primary block is associated with the redundant block via set-associative mapping.

12. (Original) The invention of Claim 1, wherein the primary block is associated with the redundant block via fully-associative mapping.

13. (Original) The invention of Claim 1, wherein the memory array comprises write-once memory cells.

14. (Original) The invention of Claim 1, wherein the memory array comprises a three-dimensional memory array of vertically-stacked field-programmable memory cells.

15. (Original) The invention of Claim 1, wherein the memory array comprises a semiconductor material.

16. (Original) The invention of Claim 1, wherein (b) is performed by a memory device comprising the memory array.

17. (Original) The invention of Claim 1, wherein (b) is performed by a host device coupled with a memory device comprising the memory array.

18. (Currently Amended) A method for providing redundancy when field programming ~~writing to~~ a memory array, the method comprising:

(a) providing a memory array comprising a primary block of memory cells and a redundant block of memory cells;

(b) attempting to field program ~~write to~~ the primary block with data ~~when field programming the memory array~~;

(c) while attempting to field program ~~write to~~ the primary block with the data, determining that an error occurred in field programming ~~writing to~~ the primary block with the data; and

(d) field programming ~~writing to~~ the redundant block with the data.

19. (Currently Amended) The invention of Claim 18 further comprising:

storing a flag in a set of memory cells allocated to the primary block in response to the error in field programming ~~writing to~~ the primary block.

20. (Original) The invention of Claim 19, wherein the flag is stored by a memory device comprising the memory array.

21. (Original) The invention of Claim 19, wherein the flag is stored by a host device coupled with a memory device comprising the memory array.

22. (Previously Amended) The invention of Claim 19 further comprising:

in response to a command to read the primary block, reading the set of memory cells allocated to the primary block; and

in response to reading the flag stored in the set of memory cells allocated to the primary block, reading the redundant block.

23. (Original) The invention of Claim 18, wherein the primary block is associated with the redundant block via direct mapping.

24. (Original) The invention of Claim 18, wherein the primary block is associated with the redundant block via set-associative mapping.

25. (Original) The invention of Claim 18, wherein the primary block is associated with the redundant block via fully-associative mapping.

26. (Original) The invention of Claim 18 further comprising:

storing an address of the primary block in a redundancy address matching circuit.

27. (Original) The invention of Claim 26 further comprising in response to a command to read the primary block:

determining that the address of the primary block is stored the redundancy address matching circuit; and

reading the redundant block.

28. (Currently Amended) The invention of Claim 18, wherein the primary block comprises a plurality of smaller blocks, and wherein the error field programming ~~writing to~~ the primary block occurs when there is an error in field programming ~~writing~~ at least one bit in one of the smaller blocks.

29. (Original) The invention of Claim 28, wherein the smaller block comprises an oct-byte and the primary block comprises a page.

30. (Currently Amended) The invention of Claim 18, wherein the error occurs when there is an error in field programming ~~writing~~ a single bit.

31. (Currently Amended) The invention of Claim 18, wherein the error occurs when there is an error in field programming ~~writing~~ two bits.

32. (Currently Amended) The invention of Claim 18, wherein the error occurs when there is an error in field programming ~~writing~~ X bits, wherein X is sufficient to introduce an error that is uncorrectable by an error protection scheme protecting at least some of the memory cells in the primary block.

33. (Original) The invention of Claim 18, wherein the memory array comprises write-once memory cells.

34. (Original) The invention of Claim 18, wherein the memory array comprises a three-dimensional memory array of vertically-stacked field-programmable memory cells.

35. (Original) The invention of Claim 18, wherein the memory array comprises a semiconductor material.

36. (Currently Amended) A memory device comprising:

a three-dimensional memory array of vertically-stacked field-programmable memory cells, the memory array comprising a primary block of memory cells and a redundant block of memory cells; and

redundancy circuitry operative to field program ~~write to~~ the redundant block in response to an error in field programming ~~writing to~~ the primary block ~~when field programming the memory array~~.

37. (Currently Amended) The invention of Claim 36, wherein the redundancy circuitry is operative to, in response to an error in field programming ~~writing to~~ the primary block, store a flag in a set of memory cells allocated to the primary block.

38. (Previously Amended) The invention of Claim 37, wherein the redundancy circuitry is further operative to, in response to a command to read the primary block, read the set of memory cells allocated to the primary block; and, in response to reading the flag stored in the set of memory cells allocated to the primary block, read the redundant block.

39. (Original) The invention of Claim 37, wherein the redundancy circuitry comprises a redundancy address matching circuit.

40. (Currently Amended) The invention of Claim 36 further comprising write circuitry operative to attempt to field program a memory cell in the primary block and, while attempting to field program the memory cell, determine that the error occurred in field programming ~~writing to~~ the primary block.

41. (Currently Amended) The invention of Claim 36 further comprising write circuitry operative to attempt to field program a memory cell in the primary block, read the memory cell

after the attempt to field program the memory cell, and determine that the error occurred in field programming ~~writing to~~ the primary block.

42. (Original) The invention of Claim 36, wherein the memory array comprises write-once memory cells.

43. (Original) The invention of Claim 36, wherein the memory array comprises a semiconductor material.

Claims 44 – 47 (Cancelled)